An Additive Approach to the Shape Synthesis of Microstrip Circuits and Antennas

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***Abstract*—An additive approach to the shape synthesis of microstrip circuits and antennas is proposed and demonstrated by example. It differs from the approaches adopted in other works on such shape synthesis.**

I. Introduction

Many passive distributed RF sub-component designs start by cascading known elementary configurations (lengths of transmission line, T-junctions, bends, coupled lines, and so on), sometimes referred to as originating from a "design library". Such library items are found in books [1,2] and journal/conference publications. Full-wave computational electromagnetics (CEM) "forward" analysis can be used to compute the performance of the assembled circuit, and this is used [3,4] in conjunction with some optimization algorithm to iteratively adjust the value of selected geometrical features – the design variables – to obtain some required electrical performance (e.g. matching, filtering, power division, phase shifting, *et cetera*). CEM forward analysis is computationally time-consuming, and so often surrogate models trained using full-wave CEM forward modelling are employed to reduce this burden in the design process. Perhaps the most familiar surrogate modelling, used in actual RF engineering practice since the early 2000's, is that based on neural networks (in other words, machine learning) of various kinds [5], and correctly not claimed to be artificial-intelligence (AI) methods [6]. The above feature-optimization based design has become a truly widely-used and successful design route – it can rightly be called the "conventional" approach.

The amount of work being done and published in just about every area of RF engineering has been steadily increasing. It is not easy to stay current with the expanding "design library," and the designer could be forgiven for wondering if something has been overlooked when deciding which parts of the circuit to feature-optimize. A complementary approach could be the use of so-called shape synthesis. Shape synthesis is the process of taking a set of desired performance metrics and using an effective algorithm to actually determine the geometry (in the present case, microstrip layout geometry) of a non-radiating or radiating circuit in order to achieve the needed performance. It does not adjust the dimensions of a set of prescribed geometrical features on pre-selected shapes (from some design library). It instead attempts to allow the electromagnetic physics to tell us what the layout needs to be under some set of externally imposed design restrictions/constraints (some of which may be of a non-electrical nature), thereby broadening the abstract "design space" compared to a conventional approach. Although work on such shape synthesis has appeared in publications for over twenty-five years, the quantity has been small relative to some other topics. A variety of such synthesis methods have been used in the design of antennas [7-15] and physical circuit components [16-21]. Despite the potential design advantages offered by such methods, these are not yet used routinely in RF engineering practice. Further work is clearly needed to improve matters to the point where shape synthesis becomes attractive in such practice. Section II briefly outlines the essence of existing shape synthesis methods in order to place the additive process introduced in the present paper into context. The steps followed by the proposed additive process are described in Section III. Section IV offers an example application of the additive shape synthesis procedure to a bandpass filter, and Section V concludes the paper.

II. Limited Review of Existing Shape Synthesis Methods

Fig.1 shows the conductor layout on top of the substrate of a fictitious single-layer microstrip circuit, imagined to be the result of some pixelation-based shape synthesis process. In order to achieve such a result, pixelation-based methods can be thought of as follows: The permissible region, namely that in which conducting material is permitted to be placed, is meshed into elements (the pixels), as indicated. Any individual pixel can be either devoid of, or occupied by, conducting material. Shape synthesis consists of iteratively adjusting the spatial distribution of conductivity values (the conductor geometry) so that the desired S-parameter values and other performance metrics, over frequency, are obtained. This is accomplished by defining (in terms of these performance measures) an objective function F_{obj}, that is a function of the conductivity distribution, and which when minimized would cause the circuit to satisfy the design specifications. Shaping procedures iteratively adjust the conductivity distribution to minimize F_{obj}. The evaluation of F_{obj} for each different distribution normally requires a CEM "forward" analysis. Precisely what the initial material distribution is depends on the "user" but is often chosen so that the permissible space is populated with conducting material of the same conductivity in all pixels. The complete shaping procedure is implemented using some scripting tool that communicates with the optimizer used and can pass candidate conductivity distributions (layouts) to the CEM engine to perform the forward analyses. The forward analysis results are fed back to the optimizer to evaluate F_{obj}. This loop is repeated until F_{obj} is sufficienty minimized. Although the shaping controller script may need to be developed *ab initio*, commercial CEM software combined with commercial or open-source optimizers can usually be exploited.

In discrete-pixelation methods the conductivity in each pixel may be either zero or the value of the conductivity of the copper foil on the printed circuit substrate (the value used in the CEM

model). The latter is often chosen as infinite (PEC), at least for the first shape synthesis run. Such "binarization" of the conductivity is desirable. One usually does not want the design to purposefully depend on a range of different conductivity values. The non-continuous binary nature of the allowed conductivity prohibits the use of gradient information on F_{obj} with respect to the conductivity distribution, and thus non-gradient optimizers are used. If fine geometrical resolution is needed, as for components (e.g. filters) with intricate frequency responses, discrete-pixelation may require too many optimization variables for the non-gradient optimizers to be effective.

In continuous-pixelation methods (usually referred to as topology optimization), the conductivity is permitted to vary continuously over some range of allowed values. This permits the use of optimizers that utilize the gradient of the objective function, and computationally resourceful ways to find such gradients ("sensitivities") with respect to the optimization variables. This allows the possibility of far more variables than discrete-pixelation methods. The drawback with conducting circuits such as microstrip, is that, for fabrication and loss-minimization reasons, a layout consisting of a range of conductivity values, and certainly areas of low conductivity, is undesirable. In order to avoid this, some way of "encouraging" binarization during shaping, and its final enforcement after completion of shaping, must be done (e.g. [9], [14]). Of course, some final automated tweaking of a design so obtained is possible and should not be considered "shameful."

In an effort to accomplish fine geometrical resolution without an inordinate number of unnecessary variables, but without the binarization concerns of continuous-pixelation, [21] proposed and implemented what was termed a subtractive shape synthesis procedure. It utilizes geometrical objects (e.g. rectangles, ellipses) whose centroid locations and dimensions are the continuous variables of the shaping process. At any stage of the shaping process the object being shaped is defined by the starting shape (permissible region filled with conductor, plus the fixed port sections) with the regions occupied by these geometrical objects removed from the starting shape. This allows one to obtain the geometrical resolution needed for high-performance RF physical circuits without there being an unmanageable number of degrees of freedom, but still without the need of a "design library". The ability to continue using non-gradient optimizers makes it possible for the designer to use a complicated F_{obj} that incorporates very realistic performance requirements and design constraints (e.g. [22]).

We here put forward the complement of subtractive shape synthesis, namely an additive shaping process. The method used in the on-going work by [23] could be classified as an additive shape synthesis one, albeit in a different context to the microstrip circuit one discussed below. In [23] a 3D antenna is constructed by assembling/intersecting 3D conducting objects (cones, circular cylinders, spheres and rectangular blocks) to create an antenna, under control of an optimizer that uses CEM forward analyses in its loop. However, the antennas involved are simple geometries with relatively undemanding requirements, so that the resulting shapes take the form of perturbations of dipole/bicone-like ones. The work in [24] can likewise be considered an additive approach (within a continuous-pixelation framework) but differs substantially from what is done here.

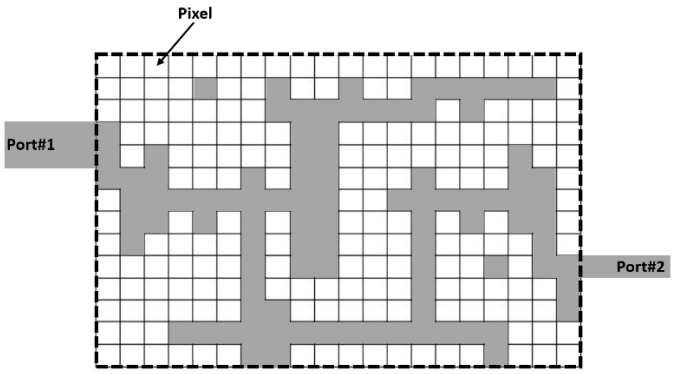

Figure 1. Permissble region (bordered by the heavy dashed black line, but which need not have a rectangular boundary) that has been divided into pixels. Those pixels occupied by conductor material are shaded. The two ports are at the ends of microstrip transmission lines, whose lengths and widths (outside of the permissible region) are assumed fixed. Pixels need not be rectangular.

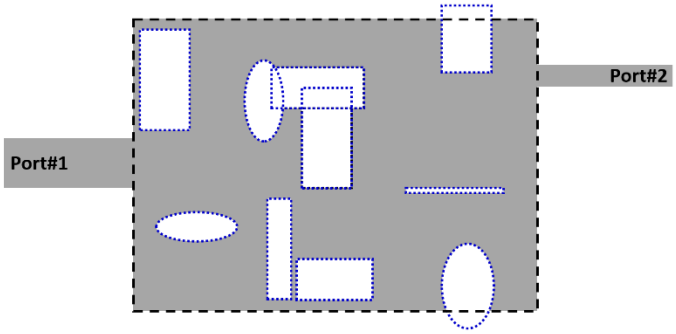

Figure 2. Permissble region (surrounded by the heavy dashed black line) that has been covered in conductor, with subtractive shapes (dotted blue boundaries) whose sizes and centroids are adjusted during the shape synthesis process. The two ports are at the ends of microstrip transmission lines, whose lengths and widths are assumed fixed.

III. An Additive Approach to Microstrip Circuit Layout Shape Synthesis

We stated above that the *subtractive* shape synthesis procedure begins with a permissible region that is entirely occupied by conductor, which is then shaped through adjustment of the size and location of the selected subtractive geometrical objects. The strategy of the proposed *additive* approach is to start with the permissible region devoid of conductor, and then use the size and location of additive elements to populate the permissible region with conductor in order to realize the shaped circuit layout. This is depicted in Fig.3, which shows the permissible region outlined by a dashed black line as before, and seven additive shapes whose size and location can be varied by the shaping process. An initial set of values for such geometrical parameters must be assigned at the commencement of any shape synthesis for it to get started.

When additive elements overlap their union simply results in a more complex conductor shape. If any part of an element extends passed the boundary of the permissible region, that part is ignored, as depicted for additive shape #7 in Fig.3. Many constraints can be embedded into the shaping algorithm via the controller script (e.g. to ensure that the additive elements do not distribute themselves in a way that allows the width of gaps, or of conducting tracks, to be less than some minimum manufacturable value). It is also possible to stipulate that certain

of the additive elements always be in physical contact with the fixed ports if desired. During the first phase of the shaping, when the shaping process "finds its feet" so to speak, one can check for galvanic continuity between the input and output ports and/or the percentage of the permissible region that is occupied by conductor. If these are not satisfied, F_{obj} can then be assigned a large value, without performing any CEM simulations. This would repeat until there is sufficient conductor present. Thereafter galvanic continuity is no longer enforced to allow the shaping to arrive at a layout that includes gaps (e.g. side-coupled lines) if it wishes to do so. If there is a requirement for galvanic continuity because the component being synthesized is part of the path of a DC-biasing current, then such a condition can of course be retained throughout. Any particular design case could further customize the strategy based on intuition in an "informed shaping" approach. In the example results to be shown here the CEM engine used is *Cadence AWR* [3]; it can permit geometry control using a shaping controller script (e.g. implemented in *Python* using the *pyawr* interface module for AWR).

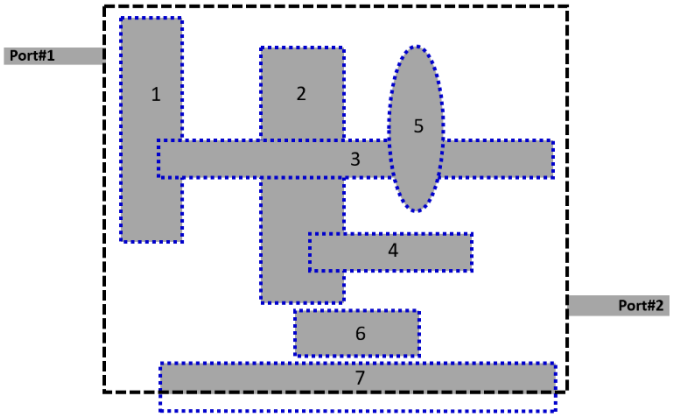

Figure 3. Permissble region (circumscribed by the heavy dashed black line) that has initially been left devoid of conductor, with seven additive rectangular objects (conductors), with their boundaries shown as dotted blue lines, and whose sizes and centroids can be adjusted during the shape synthesis process. The two ports are at the ends of microstrip transmission lines whose lengths and widths are assumed fixed.

IV. Example : Bandpass Filter

The S_{11}, S_{21} and S_{22} magnitude masks used in this band pass filter example can be inferred from Fig.5 and Fig.6, which will shortly be discussed. All three were explicitly incorporated into F_{obj} (that is, no relation between them assumed) to ensure, amongst other things, very low levels of unwanted radiation. The additive shaping process used a particle swarm optimizer (PSO). The initial resulting shape synthesized microstrip layout is that in Fig.4, obtained entirely as the result of the proposed additive shaping process. No conventional design route was used. Notice that the fixed port locations were arbitrarily selected as shown in order to demonstrate that, unlike conventional ("design library") methods that may dictate such locations, this is not so with shape synthesis procedures. The strategy was as follows: No objects were allowed to "deposit" conductor outside the permissible region. Object #1 (object #2) was fixed in place, had its width fixed, but was free to adjust its length (along the x-axis), although this length was always constrained so that it physically connects to object #4 (object #3) but may extend beyond object #4 (object #3). Apart from their connection to objects #1 and #2, objects #4 and #3 were allowed to move along the x-axis and adjust their widths and lengths. Each of objects #5 through #9 was free to adjust its centroid location, as well as its width and length. In Fig.4, boundaries have been drawn around some of the objects merely to allow all objects to be distinguished. As stated earlier, the fact that some objects (e.g. #5 and #8) end up overlapping is not a problem; their geometrical union simply represents an area occupied by a more complicated conductor shape. In other examples, we have found cases where one or more object is completely encapsulated by another, or the shaping process "quarantines" some object as an "island". These are representative of situations in which fewer additive objects are needed to meet the design performance metrics than were allotted.

In the example under consideration, the observation that the current and charge densities on object #9 are very small, and the desire to simplify the layout as much as possible, prompted us to complete the additive shape synthesis based design as follows: The pair of objects #6 and #8 was combined into a single rectangular object (of the same width everywhere). The same was done for the pair of objects #5 and #8. The electromagnetically relatively inactive object #9 was completely removed. The shaping was then restarted to regain satisfaction of the mask after the above simplifications had caused expected slight performance changes. The final performance is that shown in Fig.5 and Fig.6, with the final synthesized layout shown as the inset to Fig.5.

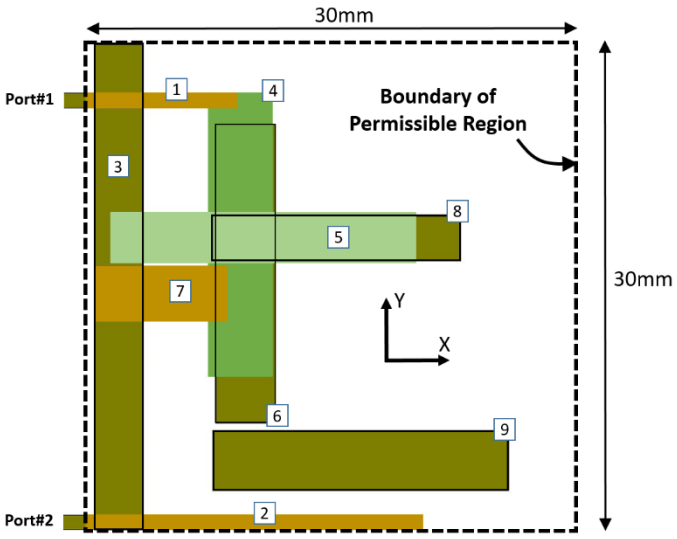

Figure 4. Bandpass filter layout obtained using additive shape synthesis. The CEM engine used a substrate (modelled on RO4835 [25]) with $\varepsilon_r = 3.739$, $tan\,\delta = 0.0037$ and height $h = 0.508$ mm. The copper trace was specified as 50 μm thick with $\sigma = 5.813 \times 10^7$ S/m.

V. Concluding Remarks

An additive approach to the shape synthesis of microstrip circuits has been proposed, and demonstrated by example. It differs from the methods adopted in other work on such shape synthesis. It contributes to on-going work on the topic of shape

synthesis in RF engineering with the goal of making the use of such a design route more routine in industry. The geometry file of the final layout (for the CEM engine AWR used) can be obtained from the last-named author on request.

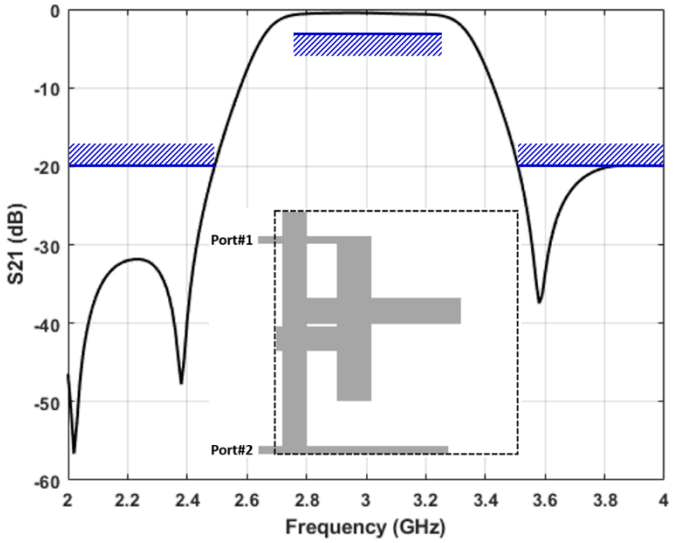

Figure 5. Computed bandpass filter S-parameter response S_{21} within the specified masks shown. The shape synthesized layout is shown as an inset. The passband is 2.75 – 3.25 GHz. The transition bands between pass- and stop-bands are 2.50 – 2.75 GHz and 3.25 – 3.50 GHz. A 3dB pass-band ripple was specified, and 20dB stop-band attenuation.

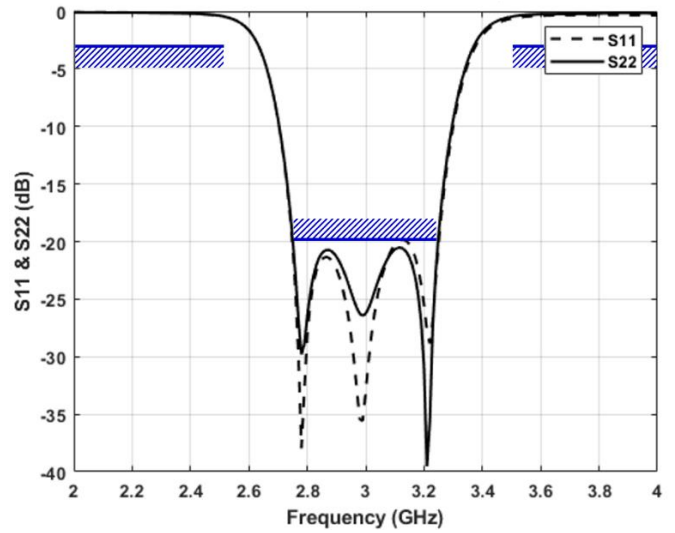

Figure 6. Computed bandpass filter S-parameter responses S_{11} and S_{22} within the specified masks shown.

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